unnecessarily protracts the prosecution. For example, after a final office action applicants can no longer amend the claims or present affidavit evidence by right, only at the discretion of the Examiner. Whereas, had the Examiner properly answered the traversals at the prior occasion, when the office action was non-final, applicants could have amended the application or entered appropriate evidence by right. At the present stage, applicants have little choice but to proceed with the present claims and evidence of record or to file an RCE, both of which unnecessarily protract the prosecution.

Applicants respectfully traverse numbered paragraph 34 of the final office action, which is not a correct statement of law or procedure.

Claims 1-8, 12-21 and 24-28 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,308,265 (Miller). Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Miller in view of U.S. Patent No. 5,960,445 (Tamori). Claims 10-11 and 22-23 are rejected as being unpatentable over Miller. Applicants respectfully traverse these rejections for the following reasons.

Applicants have amended claims 1, 6, and 12 to more clearly distinguish over the Miller reference. Specifically, applicants have clarified that some embodiments of the invention involve modifying an address bit in the execution address and maintaining the state of the address bit during a power cycle. Each of the independent claims now recites features relating to modifying an address bit of the execution address and maintaining the state of the address bit during a power cycle. Miller does not teach or suggest these features.

In order to anticipate, the reference must identically describe what is recited in the claims. As admitted in the office action, Miller discloses only setting a flag when a boot block is being updated (see Miller at col. 5, lines 65-67). The setting of a flag is different from and does not teach or suggest modifying an address bit of the execution address.

For example, some implementations of the invention may have advantages over the flag utilized in Miller. As described in connection with Fig. 4 of Miller, additional parts and operations are required to utilize the flag. Some implementations of the present invention may omit or reduce the number of extra parts or operations required by modifying and maintaining the state of the address bit of the execution address.

The office action further relies on the flag for allegedly reading on the recited maintaining the state of the address bit during a power cycle. Even assuming for the sake of argument, that the flag described in Miller corresponds in some way to modifying a bit of the execution address, it is clear that only the state of the flag is maintained in Miller. Miller does not describe that the state of the address bit is maintained during a power cycle.

In the Examiner's response to arguments, at numbered paragraph 38, the Examiner fails to directly address applicants' traversal or answer applicants' specific request to create a clear record for appeal. In the prior response, applicants specifically requested that the Examiner state for the record whether it is the position of the Examiner that the 'flag' disclosed in Miller identically describes the recited address bit of an execution address. The Examiner has declined to do so, and therefore has failed to rebut and apparently concedes this argument. If the Examiner maintains any of the rejections, applicants again respectfully request that in any further action, including any Advisory Action, that the Examiner simply state for the record whether it is the position of the Examiner that the 'flag' disclosed in Miller identically describes the recited address bit of an execution address. If the Examiner is unwilling to do this, the Examiner should concede the point and allow the case.

In numbered paragraph 38, the Examiner responds that Miller discloses, at col. 7, lines 36-42, that an address bit is inverted to point to either the first or second address according to whether a flag is set. This is erroneous. A close reading of the cited portion, and with reference to Fig. 4, shows that Miller describes inverting the state of an address line A16, not the address bit of the execution address.

In numbered paragraph 38, the Examiner further responds that "Because the flag is maintained during a power cycle the address bit is also maintained during a power cycle. This is clearly erroneous. The state of the flag does not correspond to the state of the address line A16. Miller does not teach or suggest that the state of the address line A16 is maintained during a power cycle.

Because Miller does not teach or suggest modifying an address bit of the execution address and maintaining the state of the modified address bit during a power cycle, each of independent claims 1, 6, 12, 17, 20, and 24 are each not anticipated by and are patentable over Miller. The respective dependent claims 2-5, 7-11, 13-16, 18-19, 21-23, and 25 are likewise patentable.

With respect to claim 9, Tamori, which is relied on for other features, fails to make up for the deficiencies in Miller.

With respect to claims 10-11 and 22-23, applicants first note that the office action incorrectly asserts that "Miller teaches maintaining the state of an address bit (sticky bit) following a power cycle" (emphasis added). As discussed above, Miller at most teaches maintaining the state of a flag (the sticky bit), not an address bit (or even the address line A16). The office action then admits that Miller is silent with respect to the recitations of claims 10-11, but asserts, without support from the Miller reference, that such modifications to Miller would be obvious.

In numbered paragraph 39, the Examiner states "In order for the state of a latch or flip-flop to be maintained it is inherent that power must be supplied to them." This is an improper position for at least two reasons. First, MPEP § 2112 sets forth the requirements for a rejection relying on inherency. The Examiner fails to meet the burden of proof set forth in MPEP § 2112. Second, as the Examiner is well aware, numerous forms of non-volatile circuits are well known in the art to preserve the state of a flag bit upon power failure. For example, it is possible that the state of the flag is stored in flash

memory (or other non-volatile storage) during power down and read therefrom upon power up. Because it is possible that means other than a battery may be used to maintain the state of the flag bit in Miller, it is not inherent that Miller use the claimed backup battery. Accordingly, it is not inherent or obvious that Miller would practice the particular recitations of claims 10-11. The only motivation to modify Miller in the manner suggested in the office action appears to come impermissibly from the teachings of the present specification.

In connection with claim 11, Applicants note that the cited portion describes only the use of a jumper if the inversion circuit of Fig. 4 is absent. Miller does not describe a jumper for adjusting the address bit if the backup battery fails, as recited in claim 11.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

September 6, 2005
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